



THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Harinath B. Kamepalli, Padmaraj Sanjeevarao, Chang-Jin Park  
Assignee: Sun Microsystems, Inc.  
Title: Scan Chain Verification Using Symbolic Simulation  
Serial No.: 10/790,650 Filed: March 1, 2004  
Examiner: Unknown Group Art Unit: Unknown  
Docket No.: SUN040292 Customer No.: 33438

Austin, Texas  
April 28, 2004

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INFORMATION DISCLOSURE STATEMENT

Sir:


Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, Applicants wish to call the following documents to the attention of the Examiner.

A PTO form 1449 listing these documents is enclosed.

Citation of the above documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described above; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: COMMISSIONER FOR PATENTS, PO Box 1450, Alexandria, VA 22313-1450, on April 28, 2004.



Attorney for Applicant(s)

4/28/04

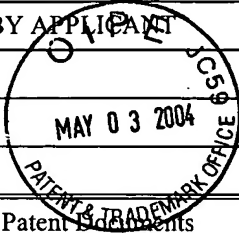
Date of Signature

Respectfully submitted,



Michael Rocco Cannatti  
Attorney for Applicant(s)  
Reg. No. 34,791

U.S. Department of Commerce, Patent and Trademark Office					Attorney Docket No.		Serial No.	
					SUN040292		10/790,650	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT					Applicant(s)			
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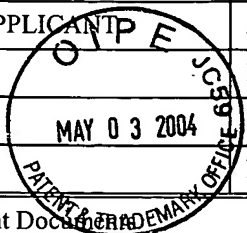
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	6,634,012	10/14/2003	Zhong et al.	716	5		
	AB	6,631,470	10/07/2003	Chang et al.	713	3		
	AC	6,574,762	06/03/2003	Karimi et al.	714	727		
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	AE	6,134,689	10/17/2000	Mateja et al.	714	736		
	AF	2003/0204802A1	10/30/2003	Sim	714	726		
	AG	2003/0131298A1	07/10/2003	Rajski et al.	714	738		
	AH	2003/0065996A1	04/03/2003	Shimada et al.	714	718		
	AI	2002/0053057A1	05/02/2002	Rajski et al.	714	738		
	AJ							
	AK							

Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
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	AM						<input type="checkbox"/>	<input type="checkbox"/>
	AN						<input type="checkbox"/>	<input type="checkbox"/>
	AO							
	AP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
AR	Takahashi, Tsuyoshi, et al., "Design Flow and Design Environment for System LSIs," Hitachi Review Vol. 48 (1999) No. 2, pp. 87-93	
AS	Kurup, Pran, et al., "Mastering HDL for formal verification," Electronics Engineer, May 1999	
AT	<a href="http://www.stridge.com/Stridge_articles/atpg_model_oview.html">http://www.stridge.com/Stridge_articles/atpg_model_oview.html</a> , "Memory ATPG Modeling and Validation Process"	

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	AN						<input type="checkbox"/>	<input type="checkbox"/>
	AO							
	AP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)	
	AR <a href="http://www.synopsys.com/products/acmgr/innlo/">http://www.synopsys.com/products/acmgr/innlo/</a> , "Former InnoLogic Systems Products"
	AS <a href="http://www.synopsys.com/products/acmgr/innlo/espvcv.html">http://www.synopsys.com/products/acmgr/innlo/espvcv.html</a> , "ESP-CV"
	AT <a href="http://www.synopsys.com/products/acmgr/innlo/esplv.html">http://www.synopsys.com/products/acmgr/innlo/esplv.html</a> , "ESP-LV"

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	AN						<input type="checkbox"/>	<input type="checkbox"/>
	AO							
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	AR	<a href="http://www.synopsys.com/products/acmgr/innlo/espbv.html">http://www.synopsys.com/products/acmgr/innlo/espbv.html</a> , "ESP-BV"						
	AS	<a href="http://www.synopsys.com/products/acmgr/innlo/ckt.html">http://www.synopsys.com/products/acmgr/innlo/ckt.html</a> , "CKT"						
	AT	<a href="http://www.synopsys.com/products/acmgr/innlo/casestudy/suncase.html">http://www.synopsys.com/products/acmgr/innlo/casestudy/suncase.html</a> , "Case Study"						
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